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APPLICATION NOTE

AN246

Transmission lines and terminations with Philips Advanced Logic families

Author: Mike Magdaluyo

February 1998

Philips
Semiconductors

PHILIPS

Transmission lines and terminations with Philips Logic families

AN246

Author: Mike Magdaluyo, Logic Products Group

INTRODUCTION

With increasing systems speeds and faster logic families, interconnect characteristics have become significant. The signal transition times of faster families can increase transmission line effects on printed circuit board traces and cables. If not taken into consideration, signal degradation can cause data errors in a system.

Previous logic families with slower rise and fall times such as LS and HCMOS were not as severely affected by this issue if line lengths were not too long. For example, an HCMOS buffer with a 5 ns edge will start exhibiting transmission line effects when a circuit board trace is longer than a foot. However, with newer families, even relatively short trace lengths become very important. This application note will briefly review transmission line concepts and evaluate transmission line effects with Philips 5 volt and 3 volt BiCMOS and CMOS logic families such as ABT, AC(T), ALVC, LVC, LVT, and ALVT.

For more detailed information on transmission lines, there are many other resources to refer to. The terms line or transmission line will refer to a cable or printed circuit trace medium and will be regarded as equivalent for electrical purposes, though their construction varies in real applications.

CRITICAL LINE LENGTH

An interconnect is considered electrically long when the round trip propagation delay of the interconnect from the driver to the load is equal to or greater than the transition time of the driver's rise or fall time. At this point, transmission line effects become significant. Using 160ps per inch as a nominal propagation delay for 50 Ω stripline medium and a nominal 0.9 ns rise time for a lightly loaded ABT driver with 15 pF loading, the critical line length is

Eq. 1

$$\text{Critical line length} = 2 \times \frac{t_{pd}}{t_r}$$

$$= 2 \times \frac{160 \text{ ps / in.}}{0.9 \text{ ns}}$$

$$= 2.8 \text{ in.}$$

For this example, traces shorter than this can be treated as lumped elements. Traces equal to or longer than this length should be modeled as distributed elements. Table 1 shows critical line lengths at various line impedances for different Philips' logic families. Assumptions are light loading of 15 pF and a nominal 8 nH per inch characteristic inductance for a PC board trace. Formulas to determine line impedance are shown in the following section.

Table 1. Maximum trace length in inches with 15pF loading

Family	tr ns	tf ns	100 Ω	70 Ω	50 Ω	35 Ω	25 Ω
HC	2.9	2.9	18.1	12.7	9.1	6.3	4.5
AHC	2.1	1.6	10.0	7.0	5.0	3.5	2.5
AC	1.2	1.7	7.5	5.3	3.8	2.6	1.9
ALS	2.7	1.7	10.6	7.4	5.3	3.7	2.7
FAST	4.0	1.4	8.8	6.1	4.4	3.1	2.2
ABT	0.9	1.2	5.6	3.9	2.8	2.0	1.4
LVT	0.8	0.6	3.8	2.6	1.9	1.3	0.9
ALVT	0.8	0.7	4.4	3.1	2.2	1.5	1.1
LVC	1.8	1.8	11.3	7.9	5.6	3.9	2.8
LV	2.9	2.9	18.1	12.7	9.1	6.3	4.5
ALVC	1.2	1.1	6.9	4.8	3.4	2.4	1.7

As you can see, using faster edge families even with relatively short traces still requires consideration of transmission line effects.

CHARACTERISTIC LINE IMPEDANCE AND CAPACITIVE LOADING

A transmission line has distributed series inductance and distributed capacitance throughout its length, and can be modeled as shown in Figure 1. The line has characteristic inductance and capacitance per unit length, l, where L_O is in Henries per inch, and C_O is in farads per inch.

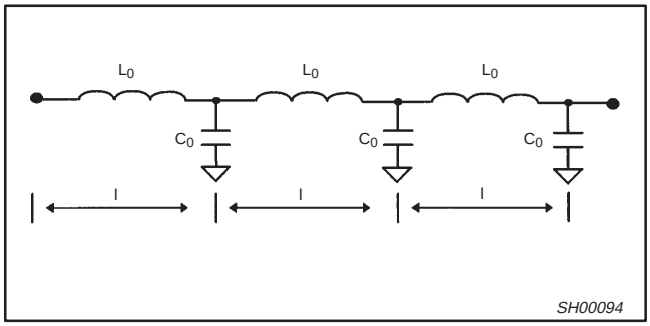

Figure 1. Circuit equivalent for a transmission line

Typical characteristic impedances on PC boards can be from 50 Ω to 100 Ω. The impedance can be determined by

Eq. 2

$$Z_O = \sqrt{\frac{L_O}{C_O}}$$

where L_0 and C_0 are the characteristic inductance and capacitance per unit length of the trace.

The line propagation delay can be determined by

Eq. 3

$$T_O = \sqrt{L_O C_O}$$

Distributed capacitive loads lower the effective impedance of a transmission line and increase the line propagation delay. Consider a bus structure with equally spaced loads of the same value as in Figure 2. The capacitors represent the input capacitance of each receiver.

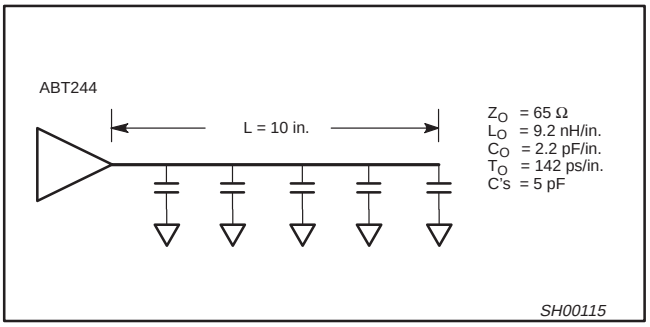

Figure 2. Equally spaced capacitive loads

If the driver's rise or fall time is longer than the electrical length of the spacing between the loads, the effects of individual capacitors distribute evenly across the waveform edge. This adds capacitance to the line's characteristic capacitance. The board interconnect at the receiver pin has capacitance also: via, connector, etc., and the values are added to the receiver's capacitance to form a lumped value. Suppose the interconnect capacitance is 5 pF, then the lumped distributed capacitance is 10 pF per every 2 inches or 5 pF per inch. The new line impedance, Z_O', can be calculated and will be

Eq. 4

$$Z_O' = \frac{Z_O}{\sqrt{1 + \frac{C_{LU}}{C_O}}}$$

$$= \frac{65\ \Omega}{\sqrt{1 + \frac{5\ \text{pF/ in.}}{2.2\ \text{pF/ in.}}}}$$

$$= 36\ \Omega$$

where C_{LU} = load capacitance per unit length, pF/in.

Likewise, the new line propagation delay will be

Eq. 5

$$T_O' = T_O \times \sqrt{1 + \frac{C_{LU}}{C_O}}$$

$$= 142\ \text{ps/in.} \times \sqrt{1 + \frac{5\ \text{pF/ in.}}{2.2\ \text{pF/ in.}}}$$

$$= 257\ \text{ps/in.}$$

Since the effective line impedance can be reduced with more loading, a driver with sufficient source and sink capability should be chosen to drive that particular impedance. This is discussed in the next section.

INCIDENT WAVE SWITCHING AND DRIVER I-V CHARACTERISTICS

When launching a pulse down the line, the driver needs sufficient current to change the voltage on the line. For TTL level input receivers, the guaranteed V_{IH} and V_{IL} levels are 2.0 V and 0.8 V. This means that the leading edge incident wave launched down the line should meet those levels to switch all receivers on the line and switch them only once. The drive current required is

Eq. 6

$$I_{AV} \text{ at } V_{OH} = \frac{V_{IH}\ \text{min} - V_{OL}\ \text{typ}}{Z_O'}$$

Eq. 7

$$I_{AV} \text{ at } V_{OL} = \frac{V_{OH}\ \text{typ} - V_{IL}\ \text{max}}{Z_O'}$$

As an example of incident wave switching capability, refer back to the bus structure in Figure 2. The effective line impedance is 34 Ω. Using Equations 6 and 7, the drive current required to switch the line is determined as follows:

$$I_{AV} \text{ at } V_{OH} = \frac{V_{IH}\ \text{min} - V_{OL}\ \text{typ}}{Z_O'}$$

$$= \frac{2\ \text{V} - 0.2\ \text{V}}{36\ \Omega}$$

$$= 50\ \text{mA}$$

and

$$I_{AV} \text{ at } V_{OL} = \frac{V_{OH}\ \text{typ} - V_{IL}\ \text{max}}{Z_O'}$$

$$= \frac{3.4\ \text{V} - 0.8\ \text{V}}{36\ \Omega}$$

$$= 72\ \text{mA}$$

ABT products are rated for +32 mA source current at 2 V and –64 mA sink current at 0.55 V. By referring to I-V curves you can determine if the dynamic drive current is enough to switch the line on the incident wave. From the following curves in Figures 3 and 4, note that the –76 mA at 2 V and +167 mA at 0.8 V satisfies the requirements in the above formulas. To compare the drive strength of other product families, Figures 5 through 9 show IOL and IOH currents for a typical '244 driver for the ABT16, ALVC, ALVT, LVC, LVT, and LVT16 families.

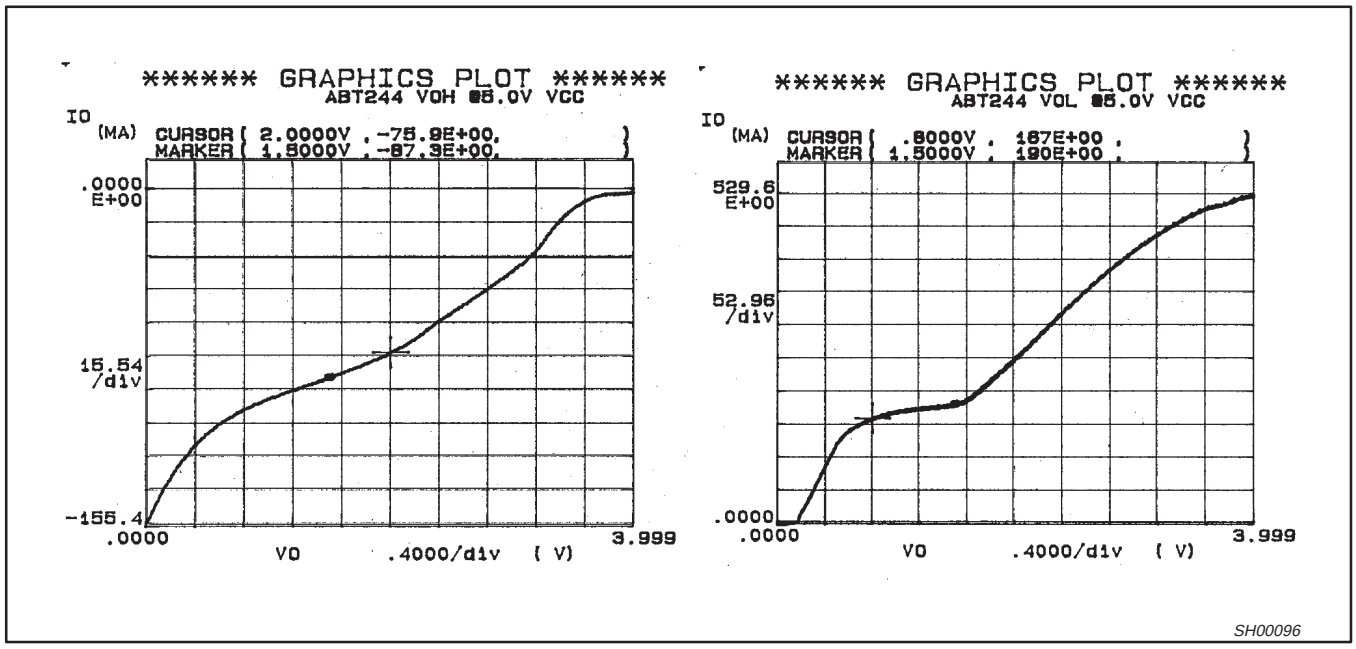

Figure 3. ABT244 I-V curves

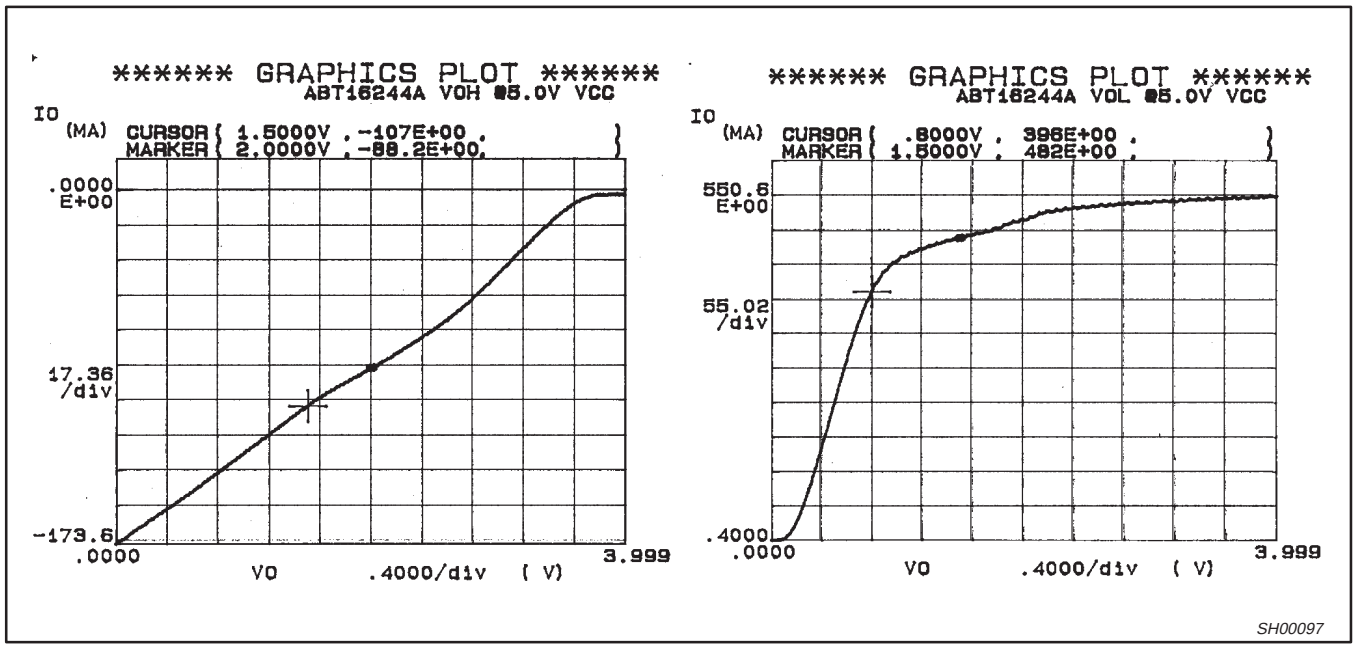

Figure 4. ABT16244 I-V curves

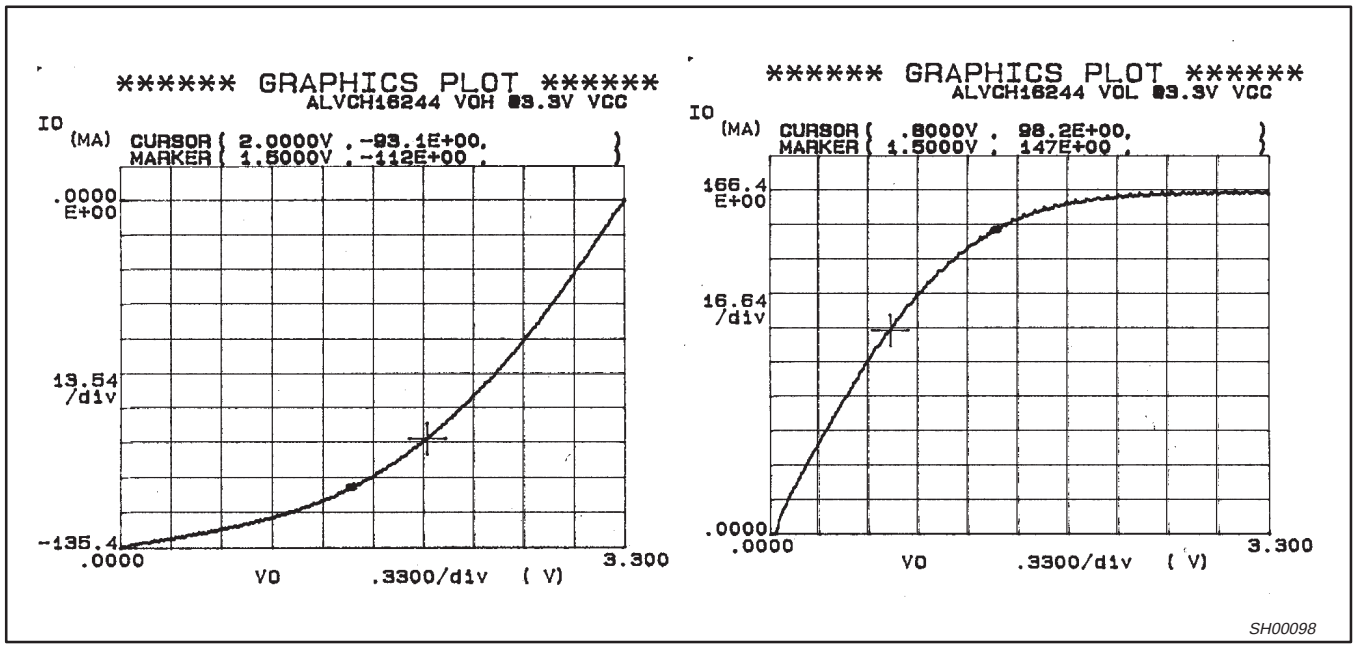

Figure 5. ALVC16244 I-V curves

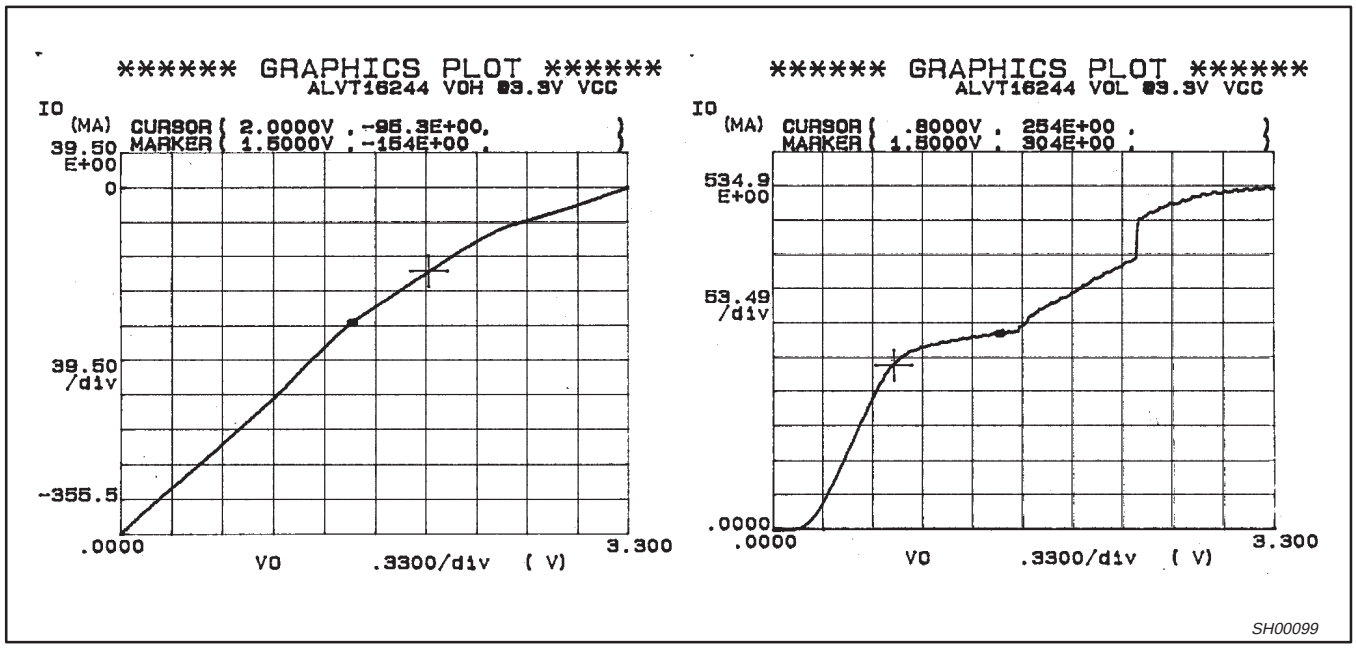

Figure 6. ALVT16244 I-V curves

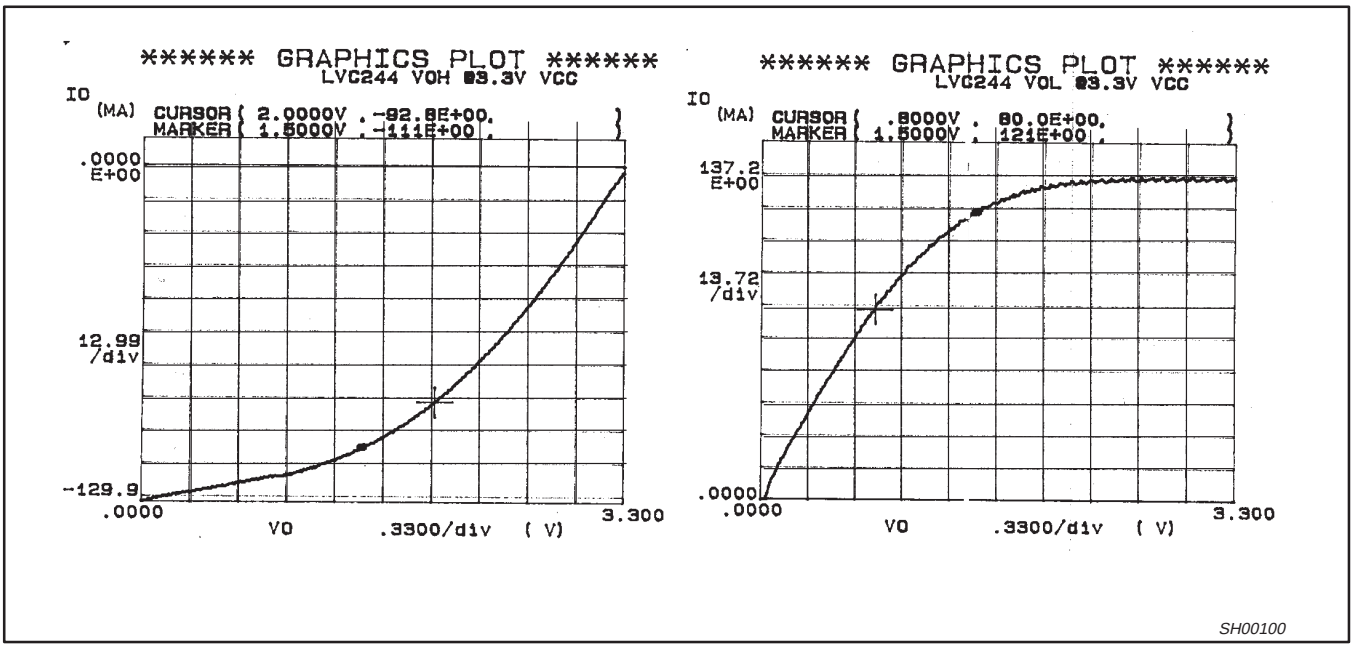

Figure 7. LVC244 I-V curves

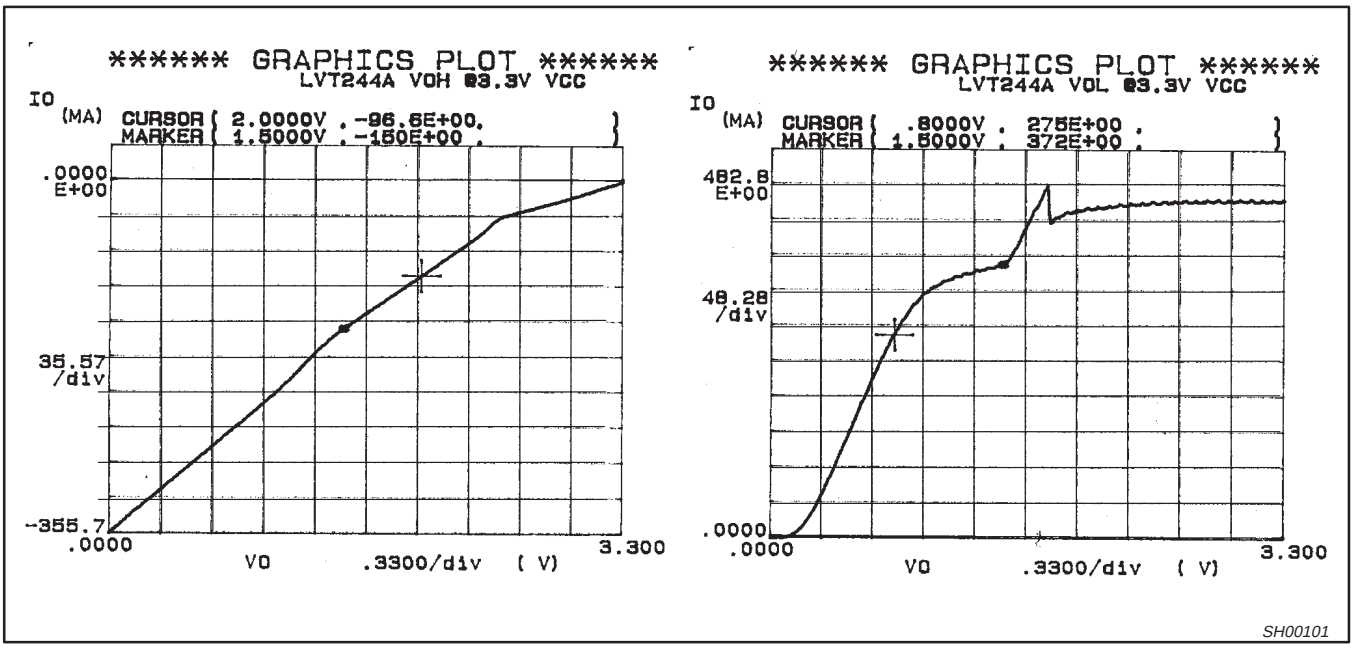

Figure 8. LVT244 I-V curves

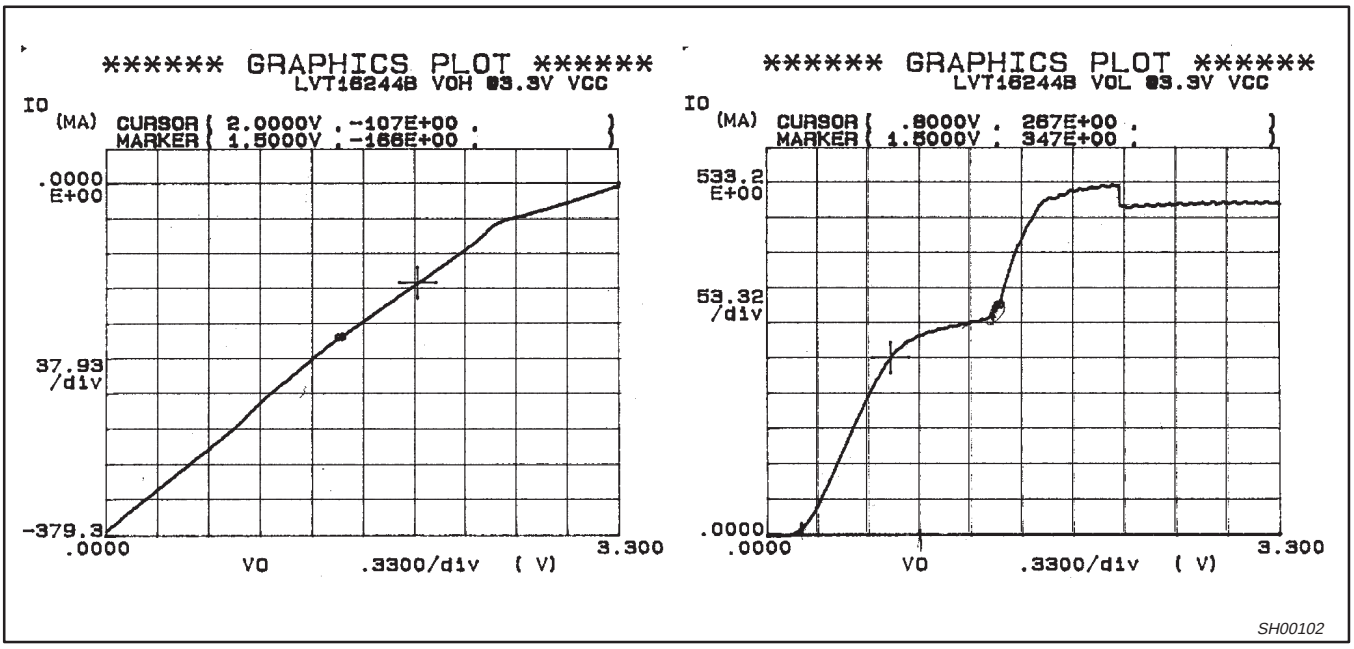

Figure 9. LVT16244 I-V curves

Based on the I-V curves, all families have good drive current in the logic high state, and ABT(16), ALVT, and LVT(16) BiCMOS families have considerably stronger drive than the other families in the logic low state. The BiCMOS families have been optimized to drive backplanes. The other CMOS families are suitable for local buses and driving point-to-point loads. The following table shows recommended minimum line impedances that can be driven by the buffer/drivers of various Philips logic families:

Table 2. Minimum line impedance for logic families

Logic Family	Minimum Z_O
ABT(16)	35 Ω
AC/ACT	50 Ω
ALS(–1)	65 Ω
FAST	50 Ω
LVT(16)	35 Ω
ALVT	35 Ω
LVC(16)	50 Ω
ALVC	50 Ω

REFLECTIONS FROM IMPEDANCE MISMATCHES

Since a driver has non-zero output impedance, its impedance along with the line impedance form a voltage divider. The incident wave launched down the line is a portion of the driver's voltage. When the wave encounters an impedance change from either the line or a receiver input, a portion of the wave is reflected back towards the driver ($V_{reflected}$) which is determined by the reflection coefficient r. The reflected portion is also added to the incident wave which continues propagating down the line ($V_{transmitted}$). The relationship of these voltages are shown in the following equations:

Eq. 8

$$\rho = \frac{(Z_{load} - Z_O)}{(Z_{load} + Z_O)}$$

Eq. 9

$$V_{reflected} = V_{incident} \times \rho$$

Eq. 10

$$V_{transmitted} = V_{incident} + V_{reflected}$$

Since driver and line impedances are usually mismatched, a reflection occurs at the driver and travels back towards the load. The reflection coefficient at the driver is determined by Equation 11:

Eq. 11

$$\rho = \frac{(Z_{driver} - Z_O)}{(Z_{driver} + Z_O)}$$

This volley of wave reflections continues, with reflections getting smaller as the signal waveform settles.

During the reflection period, the waveform may have a stairstep response—in the case of a driver's impedance higher than the line's—or it may have a "ringy" response—in the case of a driver's impedance lower than the line's. To predict the signal integrity of a waveform you can use reflection charts or Bergeron plots, but they can be cumbersome.

Another tool that is useful for evaluating these effects is SPICE models. Philips Semiconductors offers free models for our FAST, ALS, HCMOS, ABT, ABT16, ALVC, ALVT, LV, LVC, LVT, and LVT16 product families to aid in signal integrity evaluation. The models help reduce design time by eliminating time consuming efforts of reflection and Bergeron diagrams, and they also help predict signal integrity prior to board layout.

As an example, the circuit in Figure 10 was modeled and the results are shown in Figure 11. A pulse was fed into the ALVC16244 and the input and output waveforms were observed. This example illustrates the effect of reflections due to the mismatch of the driver impedance (around 10 Ω) and the transmission line.

Note that the overshoot and undershoot in Figure 11 may not be acceptable to drive other 3V device inputs or DRAM's. To reduce the overshoot and undershoot, line termination will be necessary.

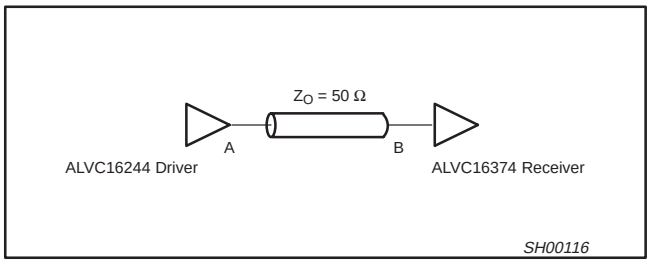

Figure 10. ALVC16244 driving ALVC16374 receiver

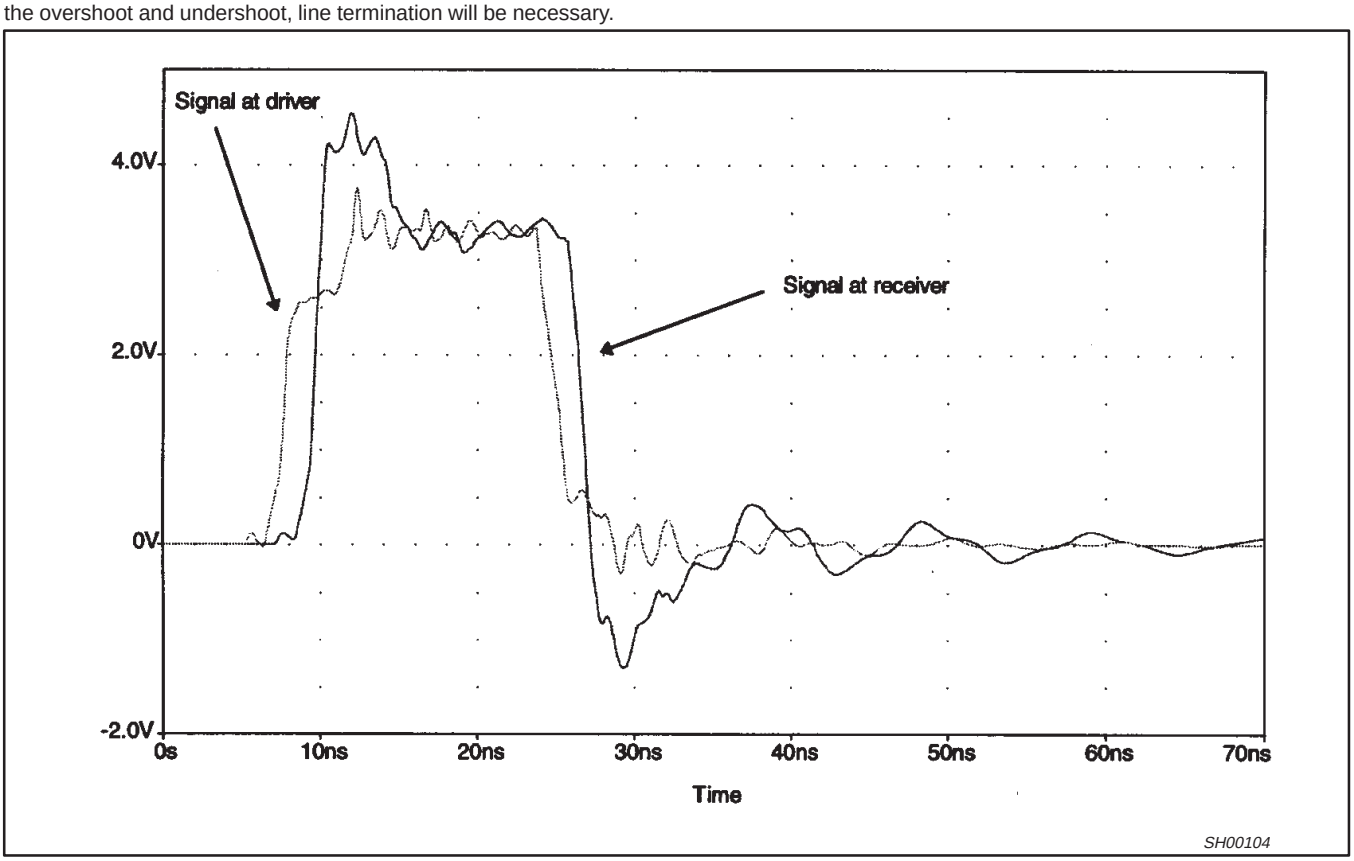

Figure 11. SPICE simulation for the circuit in Figure 10.

TERMINATION CONSIDERATIONS AND TECHNIQUES

As shown earlier, impedance mismatches between the source, line and load can cause reflections. These reflection can cause signal delays, such as the case of a stairstep type of response which requires additional line delays to reach sufficient switching threshold levels, mis-clocking from non-monotonic edges, or excess voltage/current on inputs. A signal should be terminated if it won't settle on time, if it produces overshoot or undershoot that violates the receivers input voltage or current ratings, or if it drives edge-sensitive asynchronous inputs and has non-monotonic edges. Several termination schemes can be used depending on drive current capability, power dissipation requirements, and incident wave switching requirements.

There are two basic approaches to line termination: source termination and end termination. Both schemes will result in a stable signal at the far end of the line after one line delay. Source termination, however, results in a stable signal up to two line delays for loads at intermediate points on the line and at the source. More details of each scheme follows.

Source Terminations Methods

Figure 12 shows the configuration of a source terminated daisy chain line.

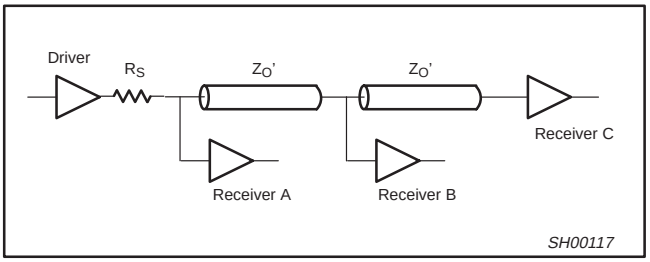

Figure 12. Source termination configuration

The concept of this termination method is to try and match the loaded line impedance with the sum of the driver output and series resistor impedances. The series resistor value is equal to Z_O' minus the driver impedance. The resistor should be located as close to the driver as possible.

Since the sum of the driver impedance and series resistor equals the line impedance, a half-height wave travels down the line from the voltage divider effect. Assuming a reflection coefficient approaching +1 at the end of the line, the reflection adds to the half-height wave, and the voltage at the last receiver is at near full amplitude. The wave amplitude at the first and intermediate receivers, however, are half-height and require up to one additional line delay for the reflected wave to reach the series terminator and add to the initial wave. Figure 13 shows a SPICE simulation of the reflections for this circuit and termination method.

Note that the last receiver is first to switch to the full signal amplitude, while the first receiver is the last to reach full amplitude. This means that any edge-sensitive asynchronous signals should be located at the end of the line. Non-monotonic edges at the beginning and intermediate points along the line could cause false clocking of devices. Also, drivers at the beginning and at intermediate points need to be able to tolerate roughly twice the settling time.

As you can see, this termination method is not very good for lines with daisy chain topologies. Source terminators work well, though, for single receiver, point-to-point loads and star type of topologies. They work well to dampen overshoot and undershoot.

Source terminators dissipate no quiescent power. The AC power dissipation can be estimated by:

Eq. 12

$$P \approx f_{2T}\left(\frac{\Delta V}{2R}\right)^2$$

where f = pulse frequency
where T = one-way line delay
ΔV = V_{OH}–V_{OL}
R = termination resistance

This approximation works if the pulse interval is greater than twice the line delay. For shorter pulse intervals, you can assume a worst case of DV/2 across the termination resistor at all times. With its low power dissipation, series termination is recommended for low voltage logic.

As mentioned previously, the sum of source impedance and the series terminator should match the loaded line impedance. Since output impedances are different in the logic low and high states, there needs to be a compromise when choosing the termination resistance. It's probably better to slightly overdrive the line by choosing a smaller resistor to ensure fast enough edge transitions to a valid logic level. Typical values in applications range from 22 Ω to 33 Ω. Philips offers ABT, ALVC, ALVT, LVC, and LVT parts with built-in series terminators that have equivalent output impedances of 30 Ω. These parts save board space by eliminating the need for a terminating resistor. Part types are designated by a "2" prefix before the part type number, e.g., 74ABT2245.

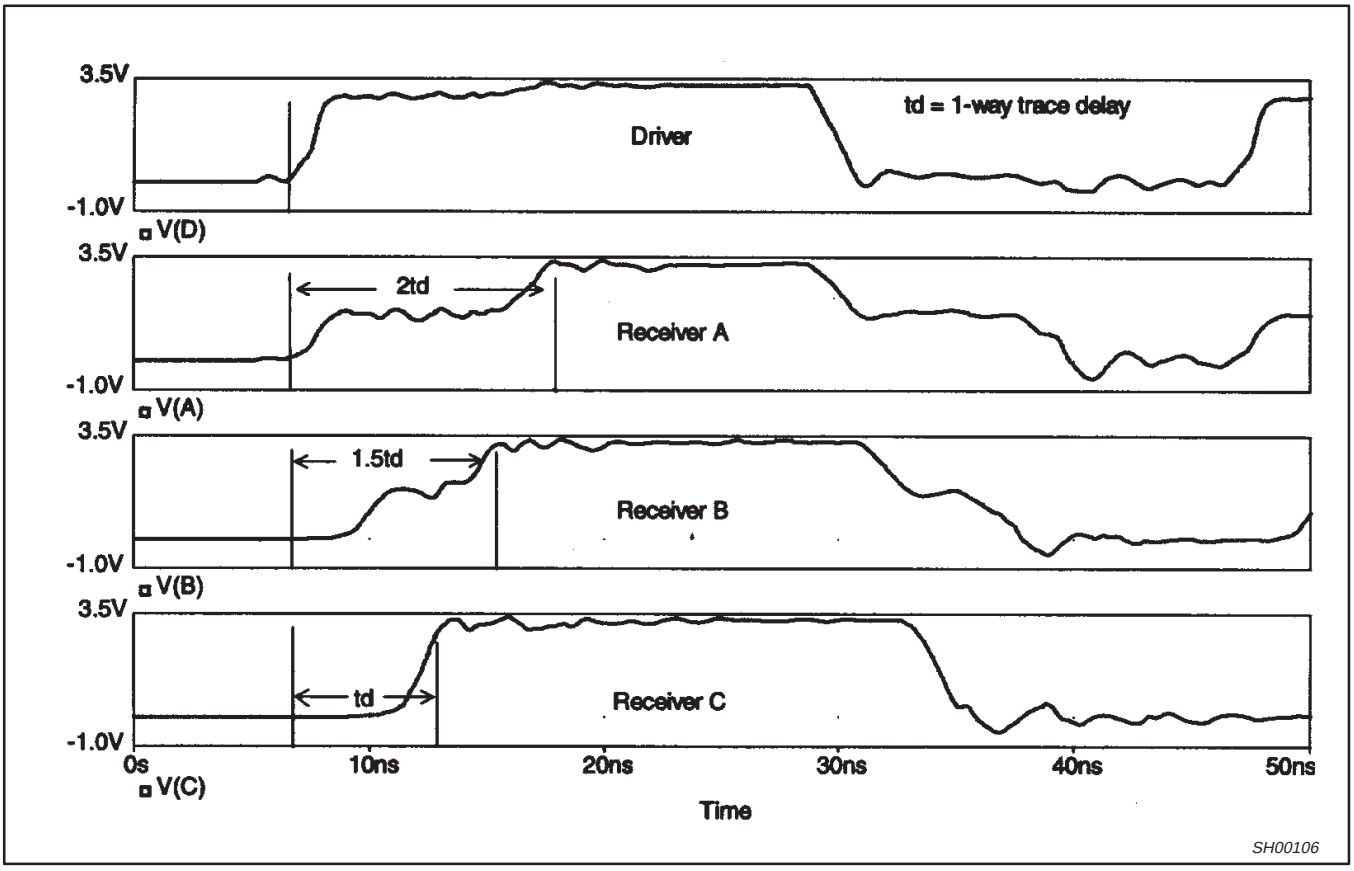

Figure 13. Reflections from source termination

Other Series Termination Schemes

Figure 14 shows a series termination used with a star stub topology.

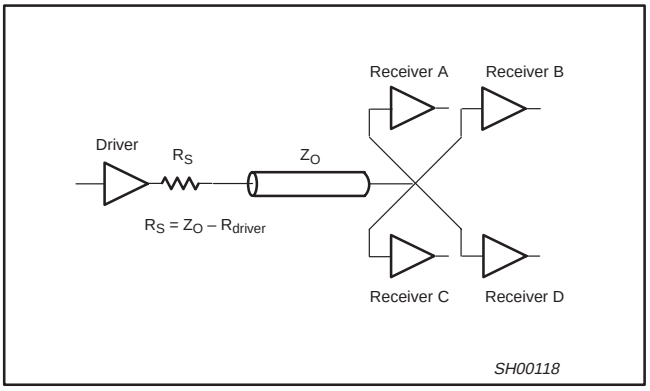

Figure 14. Series termination with star stub routing

Stub electrical lengths should be very short, about 10% of the signal edge, to prevent reflections. This method is useful for terminating clocks and other asynchronous signals if stubs are of equal length/delay. Terminating methods for some alternative star routing is shown in Figure 15.

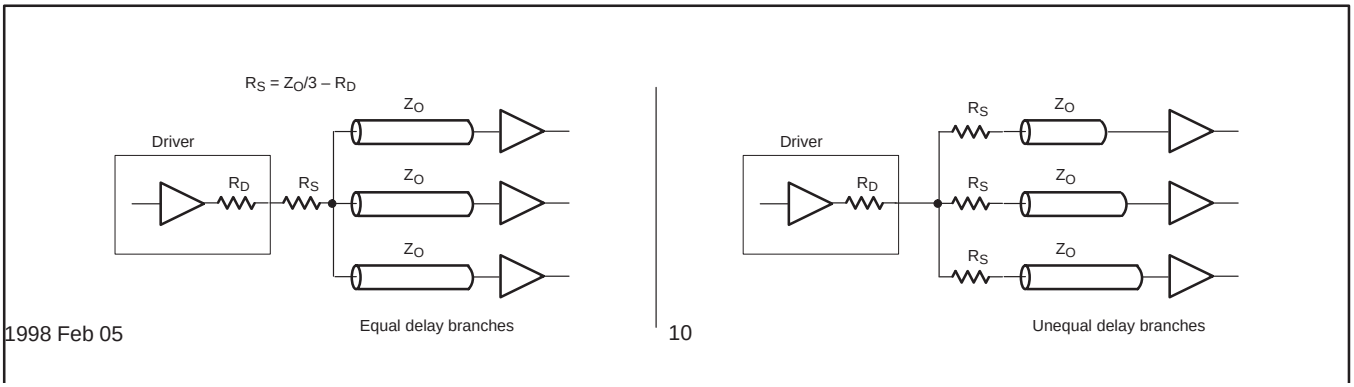

Figure 16 shows another method of series termination.

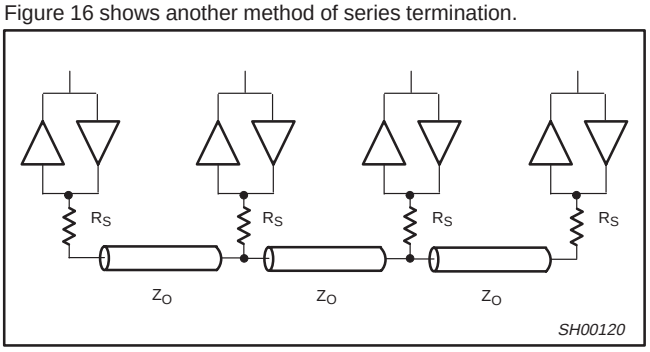

Figure 16. Series stub termination

Note that the drivers at the end will be driving RS + Z_O. Drivers in the middle should be strong enough to drive RS + Z_O/2. Again, keep stub lengths short.

End Terminations

End terminated line are recommended for distributed loads, and several methods can be used such as parallel, AC, and diode clamp methods. Figure 17 shows two parallel termination schemes.

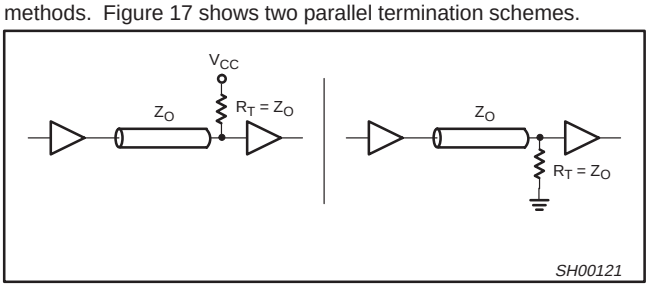

Figure 17. Parallel terminations

With this method, the termination resistance is matched to the effective line impedance. The advantage is that this method allows for incident wave switching. The disadvantages are that you need an extremely strong driver and it consumes high static power.

To reduce the drive requirements and power dissipation for this configuration, a more practical parallel Thevenin termination is shown in Figure 18 can be used.

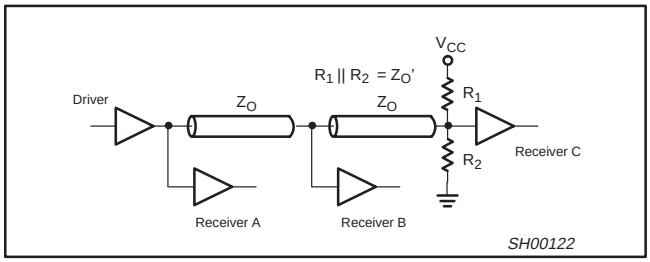

Figure 18. Daisy chain topology with split resistor Thevenin termination

This method is suitable for ABT, LVT, and ALVT families but not recommended for low voltage CMOS logic if power dissipation is a concern. The termination is placed at the end of the line as close to the receiver as possible.

If this termination technique is used on LVC and ALVC drivers, take precaution not to connect the pull-up resistor to a 5 volt supply in a mixed 3 volt/5 volt system. This can cause 5 volt supply current to flow to the 3 volt supply through the upper PMOS transistor's parasitic diode of the driver output during the active high state.

If used on a 3-State bus, avoid biasing the receiver input at its threshold switching voltage which is about 1.5 V for BiCMOS and CMOS TTL level inputs. Inputs left floating around the threshold region can consume excessive current or cause oscillations. You can use the following formula to determine values for R1 and R2 if they are not equal:

Eq. 13

$$R_1 = Z_O \frac{V_{CC}}{V_T} \text{ and } R_2 = Z_O \frac{V_{CC}}{V_{CC} - V_T}$$

where V_T = termination voltage.

A good termination voltage to choose is 2.5 V for TTL thresholds.

Assuming a 50% duty cycle, the average power dissipation of the resistors will be:

Eq. 14

$$P = 0.5 \times \left(\frac{V_{OH}^2 + V_{OL}^2}{2R_2} + \frac{(V_{CC} - V_{OH})^2 + (V_{CC} - V_{OL})^2}{2R_1} \right)$$

Another method to reduce quiescent power dissipation is AC termination shown in Figure 19. This method is recommended for distributed loads or when static power consumption is a concern.

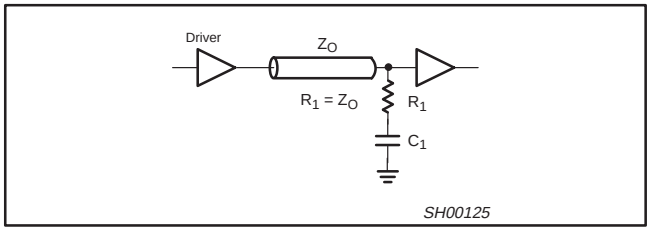

Figure 19. AC termination

No DC current flows during quiescent high or low logic levels, but an AC current path is available through C1 to terminate the line. Choose XC to be a small percentage of Z_O at the operating frequency of:

Eq. 15

$$f = \frac{1}{2T_r}$$

where T_r is the faster of the rise or fall time

Also, for DC balanced signals with 50% duty cycle, choose C such that Z_OC is much greater than the pulse period. For DC imbalanced signals, choose C such that Z_OC is much greater than the rise time but much smaller than half the pulse period.

Provided that the duty cycle is 50%, the average voltage across C1 is midway between the driver high and low output levels. R1 will also have half the voltage swing always across it. The power dissipation across R1 will be:

Eq. 16

$$P = \frac{\left(V_{OH} - \frac{V_{OL}}{2}\right)^2}{Z_O} = \frac{(V_{OH} - V_{OL})^2}{4Z_O}$$

Another method of end termination is shown in Figure 20.

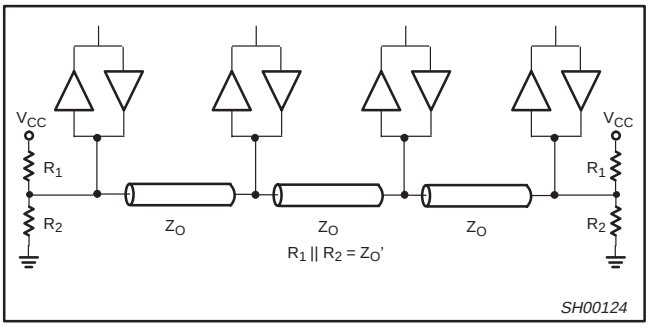

Figure 20. Party bus dual termination

The same principles should be applied to this method as in the Thevenin termination. Note that drivers will need to be strong, such as the BiCMOS devices, since they will have to drive half the value of Z_O.

The last method of end termination discussed in this paper is diode clamp termination shown in Figure 21:

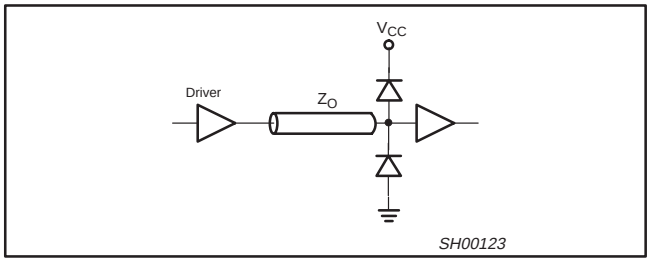

Figure 21. Diode clamp termination

The advantages are that it dissipates no power and it adds no delay to the net. The method is good to clamp overshoot and undershoot provided that it is fast enough to react to the rising or falling edge. The disadvantage is that it won't limit overshoot on 5 volt TTL drivers such as ABT. Also, it can't guarantee monotonicity on weak drivers.

CONCLUSION

Philips Semiconductors offers various advanced CMOS and BiCMOS families for high speed bus applications. This paper discussed aspects of transmission line effects with these families. Critical line length, line impedance, loading, and drive capability of different product families was examined. Impedance mismatches and reflections were discussed along with various termination solutions. Considerations of these various factors will help solve signal integrity issues in a design, and these factors need to be considered with their tradeoffs to satisfy the system design needs.

To help make design efforts easier, Philips Semiconductors offers free SPICE models for our 3V and 5V product families to aid in signal integrity evaluation. The models help reduce design time by eliminating time consuming efforts of reflection and Bergeron diagrams, and they also help predict signal integrity prior to board layout.

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Transmission lines and terminations with Philips Advanced Logic families

AN246

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